AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Claim 1 (currently amended). A computer system comprising:

a communications bus implemented in accordance with an Inter-IC bus specification;

a bus controller coupled to the communications bus;

a send machine coupled between a host processor and the bus controller; and

a first first-in first-out (FIFO) buffer coupled to the send machine and coupled between the host processor and the bus controller but not between the send machine and the bus controller.

Claim 2 (original). The computer system of claim 1, wherein the first FIFO buffer comprises means for receiving a plurality of bytes from the host processor without interrupting the host processor.

Claim 3 (original). The computer system of claim 1, wherein:

the first FIFO buffer comprises means for receiving a plurality of bytes from the host processor; and

the send machine comprises means for transmitting the plurality of bytes over the communications bus without interrupting the host processor.

Claim 4 (original). The computer system of claim 1, further comprising:

a receive machine coupled between the host processor and the bus controller; and

a second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller.

Claim 5 (original). The computer system of claim 4, wherein the receive machine comprises means for generating a message checksum for a message while the message is being received by the bus controller over the communications bus.

Claim 6 (original). The computer system of claim 1, further comprising:

means for receiving a message from the host processor;

means for attempting to send the message over the communications bus to a target device;

means for determining whether the message was received without errors by the target device; and

retry means for attempting again to send the message over the communications bus to the target device if it is determined that the message was not received without errors by the target device.

Claim 7 (original). The computer system of claim 6, wherein the retry means comprises means for attempting again to send the message over the communications bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device.

Claim 8 (original). The computer system of claim 6, wherein the retry means comprises means for attempting again to send the message over the communications bus to the target device without obtaining the message again from the host processor if it is determined that the message was not received without errors by the target device.

Claim 9 (original). The computer system of claim 1, further comprising:

busfree count means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the communications bus after the communications bus becomes available for use; and

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal.

Claim 10 (original). The computer system of claim 1, further comprising:

a byte timer coupled between the bus controller and the host processor.

Claim 11 (original). The computer system of claim 1, wherein the byte timer comprises means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed.

Claim 12 (currently amended). A computer system comprising:

a communications bus implemented in accordance with an Inter-IC bus specification;

a bus controller coupled to the communications bus;

a send machine coupled between a host processor and the bus controller, the send machine comprising means for transmitting the plurality of bytes over the communications bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine and coupled between the host processor and the bus controller but not between the send machine and the bus controller, the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the communications bus without interrupting the host processor; and

a second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller but not between the receive machine and the bus controller, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor.

Claim 13 (original). The computer system of claim 12, further comprising:

means for receiving a message from the host processor;

means for attempting to send the message over the communications bus to a target device;

means for determining whether the message was received without errors by the target device;

retry means for attempting again to send the message over the communications bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device;

busfree count means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to

access the communications bus after the communications bus becomes available for use;

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal; and

a byte timer coupled between the bus controller and the host processor, the byte timer comprising means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed.

Claim 14 (currently amended). A method for transmitting a message comprising a plurality of bytes over a communications bus implemented in accordance with an Inter-IC bus specification, the method comprising steps of:

(A) receiving at least two of the plurality bytes from a host processor; ~~and~~

(B) transmitting the at least two of the plurality of bytes over the communications bus without interrupting the host processor; and

(C) after step (B), interrupting the host processor.

Claim 15 (canceled).

Claim 16 (currently amended). The method of claim 14, further comprising a step of:

~~(C)~~(D) prior to step (B), storing the at least two of the plurality bytes in a buffer without interrupting the host processor; and

wherein step (B) comprises steps of:

(B)(1) retrieving the at least two bytes from the buffer; and

(B)(2) transmitting the at least two bytes over the bus without interrupting the host processor.

Claim 17 (currently amended). The method of claim 16, wherein step (~~C~~D) comprises a step of storing the plurality of bytes of the message in the buffer without interrupting the host processor.

Claim 18 (currently amended). A device for transmitting a message comprising a plurality of bytes over a communications bus implemented in accordance with an Inter-IC bus specification, the device comprising:

means for receiving at least two of the plurality of bytes from the host processor; ~~and~~

means for transmitting the at least two of the plurality of bytes over the communications bus without interrupting the host processor; and

means for interrupting the host processor after the means for receiving receives the at least two of the plurality of bytes from the host processor.

Claim 19 (canceled).

20 (original). The device of claim 18, further comprising:

means for storing the at least two of the plurality bytes in a buffer without interrupting the host processor before the means for transmitting transmits the at least two of the plurality of bytes over the communications bus; and

wherein the means for transmitting comprises:

means for retrieving the at least two bytes from the buffer; and

means for transmitting the at least two bytes of the message over the bus without interrupting the host processor.

Claim 21 (original). The device of claim 20, wherein the means for storing comprises means for storing the plurality of bytes of the message in the buffer without interrupting the host processor.

Claims 22-27 (canceled).

Claim 28 (original). A method for transmitting a message comprising a plurality of bytes from a source device having a first host processor to a destination device having a second host processor over a communications bus implemented in accordance with an Inter-IC bus specification, the method comprising steps of:

(A) at the source device, receiving at least two of the plurality of bytes from the first host processor;

(B) at the source device, storing the at least two of the plurality of bytes in a first buffer;

(C) at the source device, transmitting the at least two bytes of the message from the first buffer to the destination device over the communications bus without interrupting the first host processor;

(D) at the destination device, receiving the at least two bytes of the message without interrupting the second host processor;

(E) at the destination device, storing the at least two bytes in a second buffer; and

(F) at the destination device, transmitting the at least two bytes from the second buffer to the second host processor.

Claim 29 (original). The method of claim 28, wherein the step (B) comprises a step of storing the at least two of the plurality of bytes in the first buffer without interrupting the first host processor.

Claim 30 (original). The method of claim 28, wherein the step (E) comprises a step of storing the at least two of the plurality of bytes in the second buffer without interrupting the second host processor.

Claim 31 (original). A computer system comprising:

a communications bus implemented in accordance with an Inter-IC bus specification;

a bus controller coupled to the communications bus;

a receive machine coupled to the communications bus; and

a host processor coupled to the receive machine;

wherein the receive machine comprises checksum generation means for generating a message checksum for a message while the message is being received by the bus controller over the communications bus.

Claim 32 (original). The computer system of claim 31, wherein the checksum generation means comprises means for generating the message checksum without interrupting the host processor.

Claim 33 (original). A computer-implemented method comprising steps of:

(A) initializing a receive checksum;

(B) receiving a first portion of a message over a communications bus;

(C) updating the receive checksum based on the first portion of the message;

(D) receiving a subsequent portion of the message over the communications bus;

(E) updating the receive checksum based on the subsequent portion of the message; and

(F) after steps (A)-(E), transmitting the first and subsequent portions of the message to a host processor;

wherein steps (A)-(E) are performed without interrupting the host processor.

Claim 34 (original). The method of claim 33, further comprising a step of:

(G) repeating steps (D)-(E) until reception of the message is complete.

Claims 35-37 (canceled).

Claim 38 (currently amended). A device for use in a computer system including a communications bus implemented in accordance with an Inter-IC bus specification and a bus controller coupled to the communications bus, the device comprising:

busfree count storage means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the communications bus after the communications bus becomes available for use; and

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal, the arbitration means comprising:

priority means for generating the priority signal;

modifier storage means for storing a plurality of busfree count modifiers;

selection means for selecting one of the plurality of busfree count modifiers based on the priority signal; and

modification means for modifying the default busfree count based on the selected one of the plurality of busfree count modifiers to produce the arbitrated busfree count signal.

Claim 39 (canceled).

Claim 40 (original). The computer system of claim 38, wherein the modifier storage means comprises a plurality of registers.

Claim 41 (original). The computer system of claim 38, wherein the selection means comprises a multiplexer.

Claim 42 (currently amended). A computer system comprising:

a communications bus;

a bus controller coupled to the communications bus;

a send machine coupled between a host processor and the bus controller, the send machine comprising means for transmitting the plurality of bytes over the communications bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine and coupled between the host processor and the bus controller but not between the send machine and the bus controller, the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the communications bus without interrupting the host processor;

a second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller but not between the receive machine and the bus controller, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor;

means for receiving a message from the host processor;

means for attempting to send the message over the communications bus to a target device;

means for determining whether the message was received without errors by the target device;

retry means for attempting again to send the message over the communications bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device;

busfree count means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the communications bus after the communications bus becomes available for use;

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal; and

a byte timer coupled between the bus controller and the host processor, the byte timer comprising means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed.

Claim 43 (currently amended). A computer system comprising:

a communications bus;

a bus controller coupled to the communications bus;

a send machine coupled between a host processor and the bus controller, the send machine comprising means for transmitting the plurality of bytes over the communications bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine and coupled between the host processor and the bus controller but not between the send machine and the bus controller, the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the communications bus without interrupting the host processor and means for generating a message checksum for a message while the message is being received by the bus controller over the communications bus without interrupting the host processor; and

a second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller but not between

the receive machine and the bus controller, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor.

Claim 44 (currently amended). A device for use in a computer system including a communications bus and a bus controller coupled to the communications bus, the device comprising:

a send machine coupled between a host processor and the bus controller, the send machine comprising means for transmitting the plurality of bytes over the communications bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine and coupled between the host processor and the bus controller but not between the send machine and the bus controller, the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the communications bus without interrupting the host processor;

a second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller but not between the receive machine and the bus controller, the second FIFO buffer

comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor;

busfree count storage means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the communications bus after the communications bus becomes available for use; and

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal.